

Refine Search

Search Results -

Term	Documents
(17 AND 34).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	1
(L34 AND L17).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	1

Database:

US Pre-Grant Publication Full-Text Database
 US Patents Full-Text Database
 US OCR Full-Text Database
 EPO Abstracts Database
 JPO Abstracts Database
 Derwent World Patents Index
 IBM Technical Disclosure Bulletins

Search:

L39

Refine Search

Recall Text

Clear

Interrupt

Search History

DATE: Thursday, July 12, 2007 [Purge Queries](#) [Printable Copy](#) [Create Case](#)

<u>Set</u> <u>Name</u>	<u>Query</u>	<u>Hit</u> <u>Count</u>	<u>Set</u> <u>Name</u> result set
side by side			
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L39</u>	L34 and l17	1	<u>L39</u>
<u>L38</u>	L34 and l8	33	<u>L38</u>
<u>L37</u>	L34 and l7	25	<u>L37</u>
<u>L36</u>	L34 and l5	459	<u>L36</u>
<u>L35</u>	L34 and l4	96	<u>L35</u>
<u>L34</u>	l30 and register\$1 nearl2 (stack or memor\$4 or stor\$5 or ram or rom or eprom or eeprom or sram or dram)	459	<u>L34</u>
<u>L33</u>	l30 and (stack or memor\$4 or stor\$5 or ram or rom or eprom or eeprom or sram or dram)	722	<u>L33</u>
<u>L32</u>	L28 and l8	465	<u>L32</u>
<u>L31</u>	L28 and l7	29	<u>L31</u>
<u>L30</u>	L28 and l5	722	<u>L30</u>

<u>L29</u>	L28 and l4	2055	<u>L29</u>
	(single or one) near2 (instruction or command or macro near1 instruction or macroinstruction or microinstruction) near12 (plur\$7 or multipl\$7 or two or		
<u>L28</u>	dual or second) near8 (transfer\$5 or read\$3 or writ\$6 or operation\$1 or move\$1)	7908	<u>L28</u>
	(single or one) near5 (instruction or command or macro near1 instruction or macroinstruction or microinstruction) near12 (plur\$7 or multipl\$7 or two or		
<u>L27</u>	dual or second) near8 (transfer\$5 or read\$3 or writ\$6 or operation\$1 or move\$1)	13899	<u>L27</u>
<u>L26</u>	L25 and l4	3211	<u>L26</u>
	(single or one) near5 (instruction or command or macro near1 instruction or macroinstruction or microinstruction) near18 (plur\$7 or multipl\$7 or two or		
<u>L25</u>	dual or second) near10 (transfer\$5 or read\$3 or writ\$6 or operation\$1 or move\$1)	15831	<u>L25</u>
<u>L24</u>	l3 and l17	0	<u>L24</u>
<u>L23</u>	l3 and l8	6	<u>L23</u>
<u>L22</u>	l3 and l7	1	<u>L22</u>
<u>L21</u>	l3 and l5	13	<u>L21</u>
<u>L20</u>	l3 and l4	17	<u>L20</u>
	<i>DB=USPT; PLUR=YES; OP=OR</i>		
<u>L19</u>	l2 and l17	0	<u>L19</u>
	<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>		
<u>L18</u>	(717/136-143)![CCLS]	2514	<u>L18</u>
<u>L17</u>	(717/136-143)[CCLS]	2514	<u>L17</u>
<u>L16</u>	l1 and l8	32	<u>L16</u>
<u>L15</u>	l1 and l7	3	<u>L15</u>
<u>L14</u>	l1 and l5	30	<u>L14</u>
<u>L13</u>	l1 and l4	104	<u>L13</u>
<u>L12</u>	l2 and l8	15	<u>L12</u>
<u>L11</u>	l2 and l7	2	<u>L11</u>
<u>L10</u>	l2 and l5	14	<u>L10</u>
<u>L9</u>	l2 and l4	34	<u>L9</u>
<u>L8</u>	(712/200-203,225-228)![CCLS]	3118	<u>L8</u>
<u>L7</u>	(711/131,132)![CCLS]	372	<u>L7</u>
<u>L6</u>	711/131,132	0	<u>L6</u>
<u>L5</u>	(711/131-172,220-221)![CCLS]	21360	<u>L5</u>
<u>L4</u>	(712/2-300)[CCLS]	13526	<u>L4</u>
	<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>		
	L1 near45 (transfer\$5 or sent or send\$3 or mov\$3 or writ\$5 or load\$3 or stor\$4) near10 (register\$1) near35 (stack or memor\$4 or stor\$5 or ram or rom or eprom or eeprom or sram or dram)	43	<u>L3</u>
<u>L3</u>			
	L1 near45 (transfer\$5 or sent or send\$3 or mov\$3 or writ\$5 or load\$3 or stor\$4) near10 (register\$1)	70	<u>L2</u>
<u>L2</u>			
<u>L1</u>	(macro\$1 or macro near1 instruction\$1) near15 (push\$5 or pop\$5 or mov\$3)	2716	<u>L1</u>



Welcome United States Patent and Trademark Office

☐ Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "(((((((push*, pop*) <and> (transfer*, mov*, sent, send*) <and> register*)<in>met..."

Your search matched 40 of 126 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

☒ e-mail

» Search Options

[View Session History](#)
[New Search](#)

Modify Search

☐ Check to search only within this results set

Display Format:



Citation



Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

- ☐ 1. **ARES-architecture reinforcing superscalar**
 Yuh-Haur Lin; Feipei Lai; Meng-Chou Chang;
 VLSI Technology, Systems, and Applications, 1991. Proceedings of Technical Papers, 1991. Intern.
 22-24 May 1991 Page(s):338 - 343
 Digital Object Identifier 10.1109/VTSA.1991.246736
[AbstractPlus](#) | Full Text: [PDF](#)(416 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ 2. **A novel renaming scheme to exploit value temporal locality through physical register reuse**
 Jourdan, S.; Ronen, R.; Bekerman, M.; Shomar, B.; Yoaz, A.;
[Microarchitecture, 1998. MICRO-31. Proceedings. 31st Annual ACM/IEEE International Symposium](#)
 30 Nov.-2 Dec. 1998 Page(s):216 - 225
 Digital Object Identifier 10.1109/MICRO.1998.742783
[AbstractPlus](#) | Full Text: [PDF](#)(128 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ 3. **Checkpointed early load retirement**
 Kirman, N.; Kirman, M.; Chaudhuri, M.; Martinez, J.F.;
[High-Performance Computer Architecture, 2005. HPCA-11. 11th International Symposium on](#)
 12-16 Feb. 2005 Page(s):16 - 27
 Digital Object Identifier 10.1109/HPCA.2005.9
[AbstractPlus](#) | Full Text: [PDF](#)(168 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ 4. **Achieving supercomputer performance in a low pain environment**
 Egan, M.;
[Compcon Spring '90. 'Intellectual Leverage'. Digest of Papers. Thirty-Fifth IEEE Computer Society](#)
[Conference.](#)
 26 Feb.-2 March 1990 Page(s):205 - 207
 Digital Object Identifier 10.1109/CMPCON.1990.63675
[AbstractPlus](#) | Full Text: [PDF](#)(160 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ 5. **Overcoming the limitations of conventional vector processors**
 Kozyrakis, C.; Patterson, D.;
[Computer Architecture, 2003. Proceedings. 30th Annual International Symposium on](#)
 9-11 June 2003 Page(s):399 - 409

[AbstractPlus](#) | Full Text: [PDF\(311 KB\)](#) IEEE CNF
[Rights and Permissions](#)



6. Instruction-based self-testing of processor cores

Kranitis, N.; Gizopoulos, D.; Paschalis, A.; Zorian, Y.;
[VLSI Test Symposium, 2002. \(VTS 2002\). Proceedings 20th IEEE](#)
28 April-2 May 2002 Page(s):223 - 228
Digital Object Identifier 10.1109/VTS.2002.1011142

[AbstractPlus](#) | Full Text: [PDF\(408 KB\)](#) IEEE CNF
[Rights and Permissions](#)



7. A GaAs 32-bit RISC microprocessor

Harrington, D.L.; Troeger, G.L.; Gee, W.C.; Bolen, J.A.; Vogelsang, C.H.; Nicalek, T.P.; Lowe, C.M.
K.Q.; Fay, J.F.; Reeder, J.;
[Gallium Arsenide Integrated Circuit \(GaAs IC\) Symposium, 1988. Technical Digest 1988., 10th Ann](#)
6-9 Nov. 1988 Page(s):87 - 90
Digital Object Identifier 10.1109/GAAS.1988.11030

[AbstractPlus](#) | Full Text: [PDF\(248 KB\)](#) IEEE CNF
[Rights and Permissions](#)



8. A framework for parallelizing load/stores on embedded processors

Xiaotong Zhuang; Pande, S.; Greenland, J.S.;
[Parallel Architectures and Compilation Techniques, 2002. Proceedings. 2002 International Confere](#)
22-25 Sept. 2002 Page(s):68 - 79
Digital Object Identifier 10.1109/PACT.2002.1106005

[AbstractPlus](#) | Full Text: [PDF\(381 KB\)](#) IEEE CNF
[Rights and Permissions](#)



9. Optimal code generation for embedded memory non-homogeneous register architectures

Araujo, G.; Malik, S.;
[System Synthesis, 1995., Proceedings of the Eighth International Symposium on](#)
13-15 Sept. 1995 Page(s):36 - 41
Digital Object Identifier 10.1109/ISSS.1995.520610

[AbstractPlus](#) | Full Text: [PDF\(552 KB\)](#) IEEE CNF
[Rights and Permissions](#)



10. Compiler assisted dynamic management of registers for network processors

Collins, R.; Alegre, F.; Xiaotong Zhuang; Pande, S.;
[Parallel and Distributed Processing Symposium, 2006. IPDPS 2006. 20th International](#)
25-29 April 2006 Page(s):10 pp.
Digital Object Identifier 10.1109/IPDPS.2006.1639291

[AbstractPlus](#) | Full Text: [PDF\(192 KB\)](#) IEEE CNF
[Rights and Permissions](#)



11. Stream architectures - efficiency and programmability

Erez, M.;
[System-on-Chip, 2004. Proceedings. 2004 International Symposium on](#)
16-18 Nov. 2004 Page(s):41
Digital Object Identifier 10.1109/ISSOC.2004.1411141

[AbstractPlus](#) | Full Text: [PDF\(418 KB\)](#) IEEE CNF
[Rights and Permissions](#)



12. Effective software self-test methodology for processor cores

Kranitis, N.; Paschalis, A.; Gizopoulos, D.; Zorian, Y.;
[Design, Automation and Test in Europe Conference and Exhibition, 2002. Proceedings](#)
4-8 March 2002 Page(s):592 - 597
Digital Object Identifier 10.1109/DATE.2002.998361

[AbstractPlus](#) | Full Text: [PDF\(411 KB\)](#) IEEE CNF
[Rights and Permissions](#)

- ☐ **13. A fine-grained MIMD architecture based upon register channels**
Gupta, R.;
[Microprogramming and Microarchitecture, Micro 23, Proceedings of the 23rd Annual Workshop and Workshop on](#)
27-29 Nov. 1990 Page(s):28 - 37
Digital Object Identifier 10.1109/MICRO.1990.151424
[AbstractPlus](#) | Full Text: [PDF](#)(736 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ **14. Reducing the cost of branches by using registers**
Davidson, J.W.; Whalley, D.B.;
[Computer Architecture, 1990, Proceedings, 17th Annual International Symposium on](#)
28-31 May 1990 Page(s):182 - 191
Digital Object Identifier 10.1109/ISCA.1990.134524
[AbstractPlus](#) | Full Text: [PDF](#)(804 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ **15. On the Complexity of Register Coalescing**
Bouchez, Florent; Darté, Alain; Rastello, Fabrice;
[Code Generation and Optimization, 2007, CGO '07, International Symposium on](#)
11-14 March 2007 Page(s):102 - 114
Digital Object Identifier 10.1109/CGO.2007.26
[AbstractPlus](#) | Full Text: [PDF](#)(270 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ **16. Energy efficiency vs. programmability trade-off: architectures and design principles**
Robelly, J.P.; Seidel, H.; Chen, K.C.; Fettweis, G.;
[Design, Automation and Test in Europe, 2006, DATE '06, Proceedings](#)
Volume 1, 6-10 March 2006 Page(s):1 - 6
[AbstractPlus](#) | Full Text: [PDF](#)(288 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ **17. Dataflow Mini-Graphs: Amplifying Superscalar Capacity and Bandwidth**
Bracy, A.; Prahlaad, P.; Roth, A.;
[Microarchitecture, 2004, MICRO-37 2004, 37th International Symposium on](#)
04-08 Dec. 2004 Page(s):18 - 29
Digital Object Identifier 10.1109/MICRO.2004.15
[AbstractPlus](#) | Full Text: [PDF](#)(200 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ **18. Multi-log processor - towards scalable event-driven multiprocessors**
Viswanath, V.;
[Digital System Design, 2004, DSD 2004, Euromicro Symposium on](#)
31 Aug.-3 Sept. 2004 Page(s):279 - 286
Digital Object Identifier 10.1109/DSD.2004.1333288
[AbstractPlus](#) | Full Text: [PDF](#)(436 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ **19. Is state mapping essential for equivalence checking custom memories in scan-based design**
Krishnamurthy, N.; Bhadra, J.; Abadir, M.S.; Abraham, J.A.;
[VLSI Test Symposium, 2002, \(VTS 2002\), Proceedings 20th IEEE](#)
28 April-2 May 2002 Page(s):275 - 280
Digital Object Identifier 10.1109/VTS.2002.1011152
[AbstractPlus](#) | Full Text: [PDF](#)(255 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ **20. Exploring the number of register windows in ASIP synthesis**

Bhatt, V.P.; Balakrishnan, M.; Kumar, A.;

Design Automation Conference, 2002. Proceedings of ASP-DAC 2002, 7th Asia and South Pacific International Conference on VLSI Design, Proceedings.

7-11 Jan. 2002 Page(s):233 - 238

Digital Object Identifier 10.1109/ASPDAC.2002.994927

[AbstractPlus](#) | Full Text: [PDF\(352 KB\)](#) IEEE CNF

[Rights and Permissions](#)



21. Design and implementation of Web-based education tool

Imai, Y.; Tomita, S.; Inomo, H.; Furukawa, Z.; Shiraki, W.; Ishikawa, H.; Miyatake, A.;

Applications and the Internet (SAINT) Workshops, 2002. Proceedings, 2002 Symposium on

28 Jan.-1 Feb. 2002 Page(s):204 - 211

Digital Object Identifier 10.1109/SAINTW.2002.994571

[AbstractPlus](#) | Full Text: [PDF\(349 KB\)](#) IEEE CNF

[Rights and Permissions](#)



22. On-line Integrity monitoring of microprocessor control logic

Seongwoo Kim; Somani, A.K.;

Computer Design, 2001. ICCD 2001. Proceedings, 2001 International Conference on

23-26 Sept. 2001 Page(s):314 - 319

Digital Object Identifier 10.1109/ICCD.2001.955045

[AbstractPlus](#) | Full Text: [PDF\(632 KB\)](#) IEEE CNF

[Rights and Permissions](#)



23. High-level synthesis of nonprogrammable hardware accelerators

Schreiber, R.; Aditya, S.; Ramakrishna Rau, B.; Kathail, V.; Mahlke, S.; Abraham, S.; Snider, G.;

Application-Specific Systems, Architectures, and Processors, 2000. Proceedings, IEEE International

10-12 July 2000 Page(s):113 - 124

Digital Object Identifier 10.1109/ASAP.2000.862383

[AbstractPlus](#) | Full Text: [PDF\(236 KB\)](#) IEEE CNF

[Rights and Permissions](#)



24. Instruction-based system-level power evaluation of system-on-a-chip peripheral cores

Givargis, T.D.; Vahid, F.; Henkel, J.;

System Synthesis, 2000. Proceedings, The 13th International Symposium on

20-22 Sept. 2000 Page(s):163 - 169

Digital Object Identifier 10.1109/ISSS.2000.874044

[AbstractPlus](#) | Full Text: [PDF\(644 KB\)](#) IEEE CNF

[Rights and Permissions](#)



25. User-level DMA without operating system kernel modification

Markatos, E.P.; Katevenis, M.G.H.;

High-Performance Computer Architecture, 1997...Third International Symposium on

1-5 Feb. 1997 Page(s):322 - 331

Digital Object Identifier 10.1109/HPCA.1997.569696

[AbstractPlus](#) | Full Text: [PDF\(1008 KB\)](#) IEEE CNF

[Rights and Permissions](#)

[Help](#) [Contact Us](#) [Privacy](#)

© Copyright 2006 IE

Indexed by
 Inspec®

Welcome United States Patent and Trademark Office

☐ Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "(((((((push*, pop*) <and> (transfer*, mov*, sent, send*) <and> register*)<in>met..."

Your search matched 40 of 126 documents.

A maximum of **40** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

 e-mail

» Search Options

[View Session History](#)

New Search

» **Key**

IEEE JNL	IEEE Journal or Magazine
IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

Modify Search

```
(((((push*, pop*) <and> (transfer*, mov*, sent, send*) <and> register*)<in>metadata
```

Search >

☐ Check to search only within this results set

Display Format: ☒ Citation ☐ Citation & Abstract

[view selected items](#) [Select All](#) [Deselect All](#)

26. Hierarchical tiling for improved superscalar performance
Carter, L.; Ferrante, J.; Hummel, S.F.;
[Parallel Processing Symposium, 1995. Proceedings., 9th International](#)
25-28 April 1995 Page(s):239 - 245
Digital Object Identifier 10.1109/IPPS.1995.395939
[AbstractPlus](#) | Full Text: [PDF](#)(576 KB) IEEE CNF
[Rights and Permissions](#)
27. Controlling and programming the SPHINX multi-SIMD pyramid machine
Mehat, J.; Merigot, A.;
[Frontiers of Massively Parallel Computation, 1988. Proceedings., 2nd Symposium on the Frontiers](#)
10-12 Oct. 1988 Page(s):423 - 428
Digital Object Identifier 10.1109/FMPC.1988.47394
[AbstractPlus](#) | Full Text: [PDF](#)(380 KB) IEEE CNF
[Rights and Permissions](#)
28. BLITZEN: a highly integrated massively parallel machine
Blevins, D.W.; Davis, E.W.; Heaton, R.A.; Reif, J.H.;
[Frontiers of Massively Parallel Computation, 1988. Proceedings., 2nd Symposium on the Frontiers](#)
10-12 Oct. 1988 Page(s):399 - 406
Digital Object Identifier 10.1109/FMPC.1988.47460
[AbstractPlus](#) | Full Text: [PDF](#)(532 KB) IEEE CNF
[Rights and Permissions](#)
29. Topological testing
Malek, M.; Mourad, A.; Pandya, M.;
[Test Conference, 1989. Proceedings., 'Meeting the Tests of Time', International](#)
29-31 Aug. 1989 Page(s):103 - 110
Digital Object Identifier 10.1109/TEST.1989.82283
[AbstractPlus](#) | Full Text: [PDF](#)(640 KB) IEEE CNF
[Rights and Permissions](#)
30. Twin register architecture for an AI processor
Matoba, T.; Okamura, M.; Aikawa, T.; Minagawa, K.; Saito, M.; Maeda, K.; Takamiya, T.;
[Tools for Artificial Intelligence, 1989. Architectures, Languages and Algorithms., IEEE International](#)
23-25 Oct. 1989 Page(s):168 - 173
Digital Object Identifier 10.1109/TAI.1989.65317

Direct synthesis of optimized DSP assembly code from signal flow block diagrams
Powell, D.B.; Lee, E.A.; Newman, W.C.;
Acoustics, Speech, and Signal Processing, 1992. ICASSP-92., 1992 IEEE International Conference
Volume 5, 23-26 March 1992 Page(s):553 - 556 vol.5
Digital Object Identifier 10.1109/ICASSP.1992.226560

AbstractPlus | Full Text: [PDF](#)(356 KB) IEEE CNF
[Rights and Permissions](#)

33. A multithreaded multimedia processor merging on-chip multiprocessors and distributed vector processors
Mommers, F.; Mlynec, D.;
[Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on](#)
Volume 4, 30 May-2 June 1999 Page(s):287 - 290 vol.4
Digital Object Identifier 10.1109/ISCAS.1999.779998
[AbstractPlus](#) | Full Text: [PDF](#)(428 KB) [IEEE CNF](#)
[Rights and Permissions](#)

35. Reducing overheads of local communications in fine-grain parallel computation
Jin-Soo Kim; Soonhoi Ha; Chu Shik Jhon;
[Parallel Processing, 1997., Proceedings of the 1997 International Conference on](#)
11-15 Aug. 1997 Page(s):223 - 226
Digital Object Identifier 10.1109/ICPP.1997.622648
[AbstractPlus](#) | Full Text: [PDE\(376 KB\)](#) [IEEE CNF](#)
[Rights and Permissions](#)

37. Computer architecture simulation applets for use in teaching
Ibbett, R.; Mallet, F.;
Frontiers in Education, 2003, FIE 2003, 33rd Annual
Volume 2, 5-8 Nov. 2003 Page(s):F1C - 20-5 Vol.2
Digital Object Identifier 10.1109/FIE.2003.1264671
AbstractPlus | Full Text: PDE(481 KB) IEEE CNF
Rights and Permissions

- ☐ **38. Architecture and performance of the Hitachi SR2201 massively parallel processor system**
Fujii, H.; Yasuda, Y.; Akashi, H.; Inagami, Y.; Koga, M.; Ishihara, O.; Kashiya, M.; Wada, H.; Su
[Parallel Processing Symposium, 1997. Proceedings., 11th International](#)
1-5 April 1997 Page(s):233 - 241
Digital Object Identifier 10.1109/IPPS.1997.580901
[AbstractPlus](#) | Full Text: [PDF](#)(836 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ **39. A superscalar RISC processor with pseudo vector processing feature**
Shimamura, K.; Tanaka, S.; Shimomura, T.; Hotta, T.; Kamada, E.; Sawamoto, H.; Shimizu, T.; Na
[Computer Design: VLSI in Computers and Processors, 1995. ICCD '95. Proceedings., 1995 IEEE I](#)
[Conference on](#)
2-4 Oct. 1995 Page(s):102 - 109
Digital Object Identifier 10.1109/ICCD.1995.528797
[AbstractPlus](#) | Full Text: [PDF](#)(684 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ **40. An ASIC RISC-based I/O processor for computer applications**
Cates, R.L.; Farrell, J.J., III;
[Euro ASIC '90](#)
29 May-1 June 1990 Page(s):50 - 55
Digital Object Identifier 10.1109/EASIC.1990.207909
[AbstractPlus](#) | Full Text: [PDF](#)(484 KB) IEEE CNF
[Rights and Permissions](#)